JAPANESE [JP,08-265160,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS OPERATION EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

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CLAIMS

[Claim(s)]
[Claim 1] In case signal arrangement is performed and it becomes irregular by the transmitting side in the transmission system which carries out the strange recovery of the digital signal, the signal arrangement The gouy lei code of the coordinate of each I-axis Q-axis in signal arrangement of QPSK is made into a mother. It is characterized by extending so that all patterns may come out from a lower bit to a coordinate shaft center, making a Gray code coordinate, and being made, combining the bit of the Gray code coordinate of the I-axis and a Q-axis by turns, and gets over in a receiving side. The transmission system characterized by performing signal arrangement decode based on said signal arrangement.
[Claim 2] In the transmission system of trellis coding modulation (it is described as Following TCM) decode in a transmitting side Signal arrangement makes a mother the gouy lei code of the coordinate of each I-axis Q-axis in signal arrangement of QPSK. Extend so that all patterns may come out from a lower bit to a coordinate shaft center, and a Gray code coordinate is made. The transmission system characterized by decoding the recovery output to which is made, combining the bit of the Gray code coordinate of the I-axis and a Q-axis by turns, and modulated as signal arrangement of the non-encoding bit of each subset, and it restored by the receiving side using said signal arrangement.
[Claim 3] A coding means by which the coding bit of an information symbol is encoded, and the signal arrangement distribution means which considers the non-encoding bit of the output of said coding means, and said information symbol as an input, In case a modulation means to modulate said signal by which signal arrangement was carried out is had and transmitted With a signal arrangement distribution means, 0 is made in negative the high order bit of the coordinates 0 and 1 of QPSK as an extension bit in said case. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. this -- a degree -- the sending set characterized by recommending an escape further as a coordinate of an I-axis and a Q-axis, and signal arrangement having the subset which has arranged the figure of an I-axis Q-axis using alternation.
[Claim 4] The sending set according to claim 3 characterized by extending said extension bit as 1.
[Claim 5] A coding means by which the coding bit of an information symbol is encoded in a sending set, In case the signal arrangement distribution means which considers the non-encoding bit of the output of said coding means and said information symbol as an input, and a modulation means to modulate said signal by which signal arrangement was carried out are had and transmitted With a signal arrangement distribution means, 0 is added to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit in said case. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. Recommend an escape further as a coordinate of an I-axis and a Q-axis, and signal arrangement has the subset which has arranged the figure of an I-axis Q-axis using alternation, and faces it receiving the sending signal modulated and transmitted with said modulation means. this -- a degree -- A recovery means to restore to said input signal, and a decode means to divide into a non-encoding bit and a coding bit the recovery output to which it

restored with said recovery means, and to decode said divided coding bit, A representation symbol detection means to consider said divided non-encoding bit as an input, and to detect the representation symbol, A delay means by which it is delayed until said coding bit is decoded with said decode means in the output of said representation symbol detection means, Choose a non-encoding bit by considering as an input the coding bit decoded by the output of said delay means, and said decode means. Said representation symbol detection means is a receiving set characterized by being the representation symbol detection means share-ized [as opposed to / in case it has a non-encoding bit selector and the representation symbol of said non-encoding bit is detected / two or more modulation techniques].

[Claim 6] A coding means by which the coding bit of an information symbol is encoded in a sending set, In case the signal arrangement distribution means which considers the non-encoding bit of the output of said coding means and said information symbol as an input, and a modulation means to modulate said signal by which signal arrangement was carried out are had and transmitted With a signal arrangement distribution means, 0 is made in negative the high order bit of the coordinates 0 and 1 of QPSK as an extension bit in said case. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. Recommend an escape further as a coordinate of an I-axis and a Q-axis, and signal arrangement has the subset which has arranged the figure of an I-axis Q-axis using alternation, and faces it receiving the sending signal modulated and transmitted with said modulation means. this -- a degree -- A recovery means to restore to said input signal, and a decode means to divide into a non-encoding bit and a coding bit the recovery output to which it restored with said recovery means, and to decode said divided coding bit, A field judging means to consider said recovery output as an input and to judge the field on signal arrangement of the signal, A delay means by which it is delayed until said coding bit is decoded in the output of said field judging means, Said field judging means is a receiving set characterized by providing the field judging means share-ized [as opposed to / in case it has decode equipment which decodes a non-encoding bit by considering the output and said decoded coding bit of said delay means as an input and the field of said input signal is judged / two or more modulation techniques].

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is used for a multi-level-code-ized modulation and decode equipment in a digital modulation, and relates to an effective transmission system and a transmitting receiving set.
[0002]
[Description of the Prior Art] Now, as a signal configuration method of the modulation symbol of a multiple value, after carrying out Gray code arrangement of the axial seat label so that only 1 bit may be different as shown in drawing 8 (a), the configuration method of describing Q axial seat label after I axial seat label is taken.
[0003] Moreover, the signal arrangement of a coding modulation symbol by which trellis coding was carried out in order to carry out an error correction takes arrangement from which the distance between symbols in each (white round mark in drawing etc. and subset) serves as max for every value of a modulation, when the non-encoding bit which carries out a hard decision is divided into the group (subset) from whom a coding bit becomes the same at the time of decode, as shown in drawing 8 (b). Therefore, for example at the time of representation symbol detection of a trellis decode hard decision, as shown in drawing 9 , by 16QAM-TCM (TCM: trellis coding modulation), 2 bit x4 subset =8 bit and 64QAM-TCM had determined the signal arrangement which is different, respectively for every value of a modulation of a 6 bit x4 subset =24 bit representation symbol in 4 bit x4 subset =16 bit and 256 QAM-TCM.
[0004] That is, actuation of the decode system of drawing 9 is carried out to explaining with reference to the signal plot plan of drawing 10 (a) and drawing 10 (b). For example, the black dot of drawing 10 shows that by which the symbol transmitted by 16QAM-TCM was received.
[0005] A receiving symbol is divided into representation symbol detector 801-803 and BMU (branch metric unit) 807 side as a receiving side shows to drawing 9 . A representation symbol detector is a non-encoding bit (2 bits of high orders) decision unit, and BMU807 is a coding bit (2 bits of low order) decision unit.
[0006] The representation symbol detector, 801 [for example,], determines the thing nearest to a receiving symbol as a representation symbol the whole subset, as shown in drawing 10 (b). On the other hand, since a coding bit (2 bits of low order) is decoded powerfully, a sending signal is determined as the representation symbol of a subset with the decoded coding bit. A representation symbol is supplied to a shift register 805 through a selector 804. In this shift register 805, 4x2 bits of the representation symbol (2 bits of high orders) for every four subsets are delayed by Viterbi decoding delay until a coding bit is decoded.
[0007] on the other hand, in BMU807 which is a coding bit side, branch metric lambda0-lambda3 to the representation symbol of each subset are calculated (branch metric = -- distance [of each representation symbol and a receiving symbol]: -- refer to drawing 10 (b)). This count result is inputted into the Viterbi decoder 808. In the Viterbi decoder 808, the error from the possible transmission sequence which collapses using a previous count result and is decided by the configuration of coding is accumulated, and it considers as pass metric. The maximum past bit (the maximum past bit in pass memory) of the probable pass is outputted as a Viterbi

decoding bit among this pass metric pass (this decode output has high dependability). A Viterbi decoding result turns into the result, i.e., the output of 1 bit, before collapsing and encoding by the transmitting side. However, on the other hand, a non-encoding bit must be chosen. Therefore, after encoding by collapsing and collapsing with an encoder 809 again, the non-encoding bit is chosen by the selector 806.

[0008]

[Problem(s) to be Solved by the Invention] Since the above-mentioned signal arrangement of the conventional modulation symbol changed with values of a modulation, at the time of trellis decode, it had to detect the representation symbol from the signal arrangement which is representation symbol detection in decode of a non-encoding bit, and is different for every value of a modulation, and needed the big memory as a ROM.

[0009] Then, this invention aims at the coded signal arrangement equipment which can make memory small by not depending signal arrangement and unifying it into the value of a modulation, and making decode equipment and the signal-processing approach offer.

[0010]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the transmission approach by signal arrangement of this invention In case signal arrangement is performed and it becomes irregular by the transmitting side, the signal arrangement The gouy lei code of the coordinate of each I-axis Q-axis in signal arrangement of QPSK is made into a mother. It is characterized by extending so that all patterns may come out from a lower bit to a coordinate shaft center, making a Gray code coordinate, and being made, combining the bit of the Gray code coordinate of the I-axis and a Q-axis by turns, and gets over in a receiving side. Signal arrangement decode is performed based on said signal arrangement.

[0011]

[Function] Since what was constituted as mentioned above can realize signal arrangement of the unification corresponding to the value of various modulations, the miniaturization of the memory (ROM) in the part concerning signal arrangement of it is attained.

[0012]

[Example] Hereafter, it explains, referring to a drawing about the example of this invention. Drawing 1 is the non-encoding signal plot plan common to 16QAM and 64QAM made based on signal arrangement of QPSK. This signal arrangement technique is as stating below.

[0013] First, when it takes notice of I axial seat label in signal arrangement of QPSK of drawing 1 (a), Gray code coordinates are 0 and 1. The figure which adds zero before this figure (dotted-line part in drawing (a)), and is set to 00 and 01 is made, and as this figure is inserted, the figure of [becoming Gray code] 10, 00, 01, and 11 is made from the figure which begins from 1. this -- a degree -- assigning on an I-axis Q-axis as a coordinate of high 16QAM of a dimension, signal arrangement of a symbol location arranges what combined the figure of an I-axis Q-axis by turns (drawing 1 (b)). As for four main symbols, the arrangement as which all patterns are expressed 2 bits of low order by 00 can be taken by doing in this way, as for 2 bits of high orders.

[0014] The thing made to extend to 64QAM by the same technique is shown in drawing 2 . If this is seen, 4 bits of low order of the part enclosed with the dotted line in drawing will serve as Gray code signal arrangement of 16QAM. Moreover, if it sees about 2 bits of low order, four symbols near a core will serve as signal arrangement of QPSK. Thus, it is not based on a modulation technique but signal arrangement can be shared between using the number of bits which suited the modulation technique from the lower bit.

[0015] Similarly, 256QAM and the escape beyond it are also possible, and the method not more than it (QPSK16QAM, 64QAM) can share them. Drawing 3 is the signal plot plan which took the arrangement which 2 bits of high orders come out of main 4 SHISHIBORU, and all patterns come out of 2 bits of low order by 11 in drawing 1 of common to 16QAM and 64QAM not encoding. Drawing 4 shows the signal arrangement which extended signal arrangement of drawing 3 further.

[0016] Drawing 5 is the process in which the signal plot plan of coding common to 16QAM-TCM and 64QAM-TCM is created by making signal arrangement of drawing 1 into a subset. This is applied to signal arrangement of 64QAM-TCM as a subset that drawing 5 (a) in which signal

arrangement was carried out by the technique of drawing 1 is not encoded (drawing 5 (b)), while other three subsets rotate 90 degrees at a time, it is arranged, it adds the coding bits 00, 01, 10, and 11 to each from low order, and a signal plot plan is carried out to it (drawing 6).
[0017] If it does in this way, in signal arrangement of drawing 6 , mapping of 4x4 by the side of the core of a shaft (inside of the dotted line in drawing) is 16QAM-TCM, and the distance of the symbols which form a subset can take the distance as before. Signal arrangement possible [256 QAM-TCM and the escape beyond it] and common to the method not more than it (64QAM, 16QAM, QPSK) can be made by the same technique.
[0018] Thus, by not depending signal arrangement and unifying it into a modulation technique, the ROM memory of trellis coding decode equipment as shown in drawing 7 (a), (b), and (c) is reducible.
[0019] Drawing 7 (a) is the block diagram showing the configuration of drawing 5 and the trellis coding equipment using signal arrangement of drawing 6 . A coding bit collapses the information symbol which consists of a non-encoding bit and a coding bit, and after being inputted into an encoder 01 and encoding, it is inputted into the signal arrangement distributor 02. Although the output by which signal arrangement distribution were carried out is transmitted in the signal arrangement distributor 02, even if it does not prepare signal arrangement distribution ROM about 16QAM, 64QAM, and each 256QAM, signal arrangement distribution ROM can use the same thing by using signal arrangement of drawing 5 and drawing 6 according to the input number of bits.
[0020] Drawing 7 (b) is the block diagram showing the configuration of the trellis decode equipment by representation symbol detection. Input signals Id and Qd are divided into a non-encoding bit and a coding bit, a non-encoding bit is inputted into the representation symbol detector 03, and a hard decision is carried out for every subbit. In the representation symbol detector 03, 6 bit x4 of representation symbols judged subset is outputted. The output is delayed in a shift register 04 until a coding bit is decoded.
[0021] On the other hand, a coding bit is powerfully decoded by the Viterbi decoder 06 using the count result by BMU(branch metric unit) 08. While the decode output outputted from this Viterbi decoder 06 is outputted to the output section, it is collapsed in order to choose a non-encoding bit, and recoding is carried out with an encoder 07. On the other hand, the output of a shift register 04 is inputted into the non-encoding bit selector 05. the non-encoding bit selector 05 -- setting -- the point -- collapsing -- the representation symbol corresponding to the coding bit by which recoding was carried out is chosen, and it is outputted as decode data after that.
[0022] In addition, he uses only 2 bits only of low order of a non-encoding bit, and is trying to use [in the case of 16QAM-TCM] only 4 bits only of non-encoding bit low order at this time in the case of 64QAM-TCM.
[0023] Since according to the above configuration it does not depend on the value of a modulation but a symbol can be detected from the same signal arrangement in the case of representation symbol detection, ROMs are reducible. Drawing 7 (c) is the block diagram by field judging showing the configuration of trellis decode equipment. Input signals Id and Qd are divided into a non-encoding bit and a coding bit, and a non-encoding bit is inputted into the field judging machine 13. This field judging machine 13 judges and outputs the field of an input signal. It goes into a shift register 14 and the output is delayed until a coding bit is decoded.
[0024] On the other hand, while a coding bit is powerfully decoded by the Viterbi decoder 16 and is outputted to the output section using the count result by BMU(branch metric unit) 18, in order to choose a non-encoding bit, recoding of it is carried out with the convolutional code-ized vessel 17. On the other hand, the output of a shift register 14 is inputted into the non-encoding bit selector 15. the non-encoding bit selector 15 -- setting -- the point -- collapsing -- the representation symbol corresponding to the coding bit by which recoding was carried out is chosen, and it is outputted as decode data after that.
[0025] In addition, at this time, in the case of 16QAM-TCM, only 2 bits only of low order of a non-encoding bit are used, and, in the case of 64QAM-TCM, only 4 bits only of non-encoding bit low order are used. Since it does not depend on the value of a modulation but a field judging can be carried out from the same signal arrangement until it results [from a field judging] in a non-

encoding bit decoder according to the above configuration, ROMs are reducible.
[0026] As described above, from the coordinate of the I-axis in signal arrangement of QPSK, and each Q-axis, the signal configuration method of this invention extends a Gray code coordinate so that all patterns may come out from a lower bit to the core of a shaft, and makes it a summary to have the signal arrangement same from QPSK to 256QAM by that I and the technique of combining the figure of a Q-axis by turns.
[0027] Namely, a coding means by which the signal arrangement equipment by the side of coding of this invention encodes the coding bit of an information symbol, It has the signal arrangement distribution means which considers the non-encoding bit of the coding output of said coding means, and said information symbol as an input. With said signal arrangement distribution means 0 is added and extended to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit. the figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 -- making -- this -- a degree -- an escape is further recommended as a coordinate of an I-axis and a Q-axis, and it is characterized by making signal arrangement into the subset which has arranged the figure of an I-axis Q-axis using alternation.
[0028] Moreover, when the coding bit of an information symbol is encoded and the signal arrangement distribution of the non-encoding bit of this coding output and said information symbol are carried out, the decode equipment of this invention 0 is added and extended to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. this -- a degree -- with the means which recommends an escape further as a coordinate of an I-axis and a Q-axis, makes signal arrangement the subset which has arranged the figure of an I-axis Q-axis using alternation, receives such an input signal, and is divided into said non-encoding bit and a coding bit A decode means to decode said divided coding bit, and a representation symbol detection means to consider said divided non-encoding bit as an input, and to detect the symbol, A delay means by which it is delayed until said coding bit is decoded with said decode means in the output of said representation symbol detection means, It has the non-encoding bit selector which chooses a non-encoding bit by considering as an input the coding bit decoded with the output of said delay means, and said decode means. In case the representation symbol of a non-encoding bit is detected, said representation symbol detection means is equipped with the representation symbol detector share-ized to said two or more modulation techniques.
[0029] Moreover, when the coding bit of an information symbol is encoded and the signal arrangement distribution of the non-encoding bit of this coding output and said information symbol are carried out, the decode equipment of this invention 0 is added and extended to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. this -- a degree -- with the means which recommends an escape further as a coordinate of an I-axis and a Q-axis, makes signal arrangement the subset which has arranged the figure of an I-axis Q-axis using alternation, receives such an input signal, and is divided into said non-encoding bit and a coding bit A decode means to decode said divided coding bit, and a field judging means to consider said divided non-encoding bit as an input, and to judge the field on signal arrangement, A delay means by which it is delayed until said coding bit is decoded with said decode means in the output of said field judging means, It has a decode means to decode a non-encoding bit by considering the output and said decoded coding bit of said delay means as an input. As said field judging means In case the non-encoding bit as an output of said delay means is decoded using the output by which coding decode was carried out, the field judging machine share-ized to two or more modulation techniques is used.
[0030]
[Effect of the Invention] By arranging so that all patterns may come out from a lower bit to a coordinate shaft center in signal arrangement according to this invention, as explained above, signal arrangement corresponding to the value of two or more modulations can be realized, and ROM can be made small.

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TECHNICAL FIELD

[Industrial Application] This invention is used for a multi-level-code-ized modulation and decode equipment in a digital modulation, and relates to an effective transmission system and a transmitting receiving set.
[0002]

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PRIOR ART

[Description of the Prior Art] Now, as a signal configuration method of the modulation symbol of a multiple value, after carrying out Gray code arrangement of the axial seat label so that only 1 bit may be different as shown in drawing 8 (a), the configuration method of describing Q axial seat label after I axial seat label is taken.

[0003] Moreover, the signal arrangement of a coding modulation symbol by which trellis coding was carried out in order to carry out an error correction takes arrangement from which the distance between symbols in each (white round mark in drawing etc. and subset) serves as max for every value of a modulation, when the non-encoding bit which carries out a hard decision is divided into the group (subset) from whom a coding bit becomes the same at the time of decode, as shown in drawing 8 (b). Therefore, for example at the time of representation symbol detection of a trellis decode hard decision, as shown in drawing 9 , by 16QAM-TCM (TCM: trellis coding modulation), 2 bit x4 subset =8 bit and 64QAM-TCM had determined the signal arrangement which is different, respectively for every value of a modulation of a 6 bit x4 subset =24 bit representation symbol in 4 bit x4 subset =16 bit and 256 QAM-TCM.

[0004] That is, actuation of the decode system of drawing 9 is carried out to explaining with reference to the signal plot plan of drawing 10 (a) and drawing 10 (b). For example, the black dot of drawing 10 shows that by which the symbol transmitted by 16QAM-TCM was received.

[0005] A receiving symbol is divided into representation symbol detector 801-803 and BMU (branch metric unit) 807 side as a receiving side shows to drawing 9 . A representation symbol detector is a non-encoding bit (2 bits of high orders) decision unit, and BMU807 is a coding bit (2 bits of low order) decision unit.

[0006] The representation symbol detector, 801 [for example,], determines the thing nearest to a receiving symbol as a representation symbol the whole subset, as shown in drawing 10 (b). On the other hand, since a coding bit (2 bits of low order) is decoded powerfully, a sending signal is determined as the representation symbol of a subset with the decoded coding bit. A representation symbol is supplied to a shift register 805 through a selector 804. In this shift register 805, 4x2 bits of the representation symbol (2 bits of high orders) for every four subsets are delayed by Viterbi decoding delay until a coding bit is decoded.

[0007] on the other hand, in BMU807 which is a coding bit side, branch metric lambda0-lambda3 to the representation symbol of each subset are calculated (branch metric = -- distance [of each representation symbol and a receiving symbol]: -- refer to drawing 10 (b)). This count result is inputted into the Viterbi decoder 808. In the Viterbi decoder 808, the error from the possible transmission sequence which collapses using a previous count result and is decided by the configuration of coding is accumulated, and it considers as pass metric. The maximum past bit (the maximum past bit in pass memory) of the probable pass is outputted as a Viterbi decoding bit among this pass metric pass (this decode output has high dependability). A Viterbi decoding result turns into the result, i.e., the output of 1 bit, before collapsing and encoding by the transmitting side. However, on the other hand, a non-encoding bit must be chosen. Therefore, after encoding by collapsing and collapsing with an encoder 809 again, the non-encoding bit is chosen by the selector 806.

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EFFECT OF THE INVENTION

[Effect of the Invention] By arranging so that all patterns may come out from a lower bit to a coordinate shaft center in signal arrangement according to this invention, as explained above, signal arrangement corresponding to the value of two or more modulations can be realized, and ROM can be made small.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the above-mentioned signal arrangement of the conventional modulation symbol changed with values of a modulation, at the time of trellis decode, it had to detect the representation symbol from the signal arrangement which is representation symbol detection in decode of a non-encoding bit, and is different for every value of a modulation, and needed the big memory as a ROM.
[0009] Then, this invention aims at the coded signal arrangement equipment which can make memory small by not depending signal arrangement and unifying it into the value of a modulation, and making decode equipment and the signal-processing approach offer.

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MEANS

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the transmission approach by signal arrangement of this invention In case signal arrangement is performed and it becomes irregular by the transmitting side, the signal arrangement The gouy lei code of the coordinate of each I-axis Q-axis in signal arrangement of QPSK is made into a mother. It is characterized by extending so that all patterns may come out from a lower bit to a coordinate shaft center, making a Gray code coordinate, and being made, combining the bit of the Gray code coordinate of the I-axis and a Q-axis by turns, and gets over in a receiving side. Signal arrangement decode is performed based on said signal arrangement.

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OPERATION

[Function] Since what was constituted as mentioned above can realize signal arrangement of the unification corresponding to the value of various modulations, the miniaturization of the memory (ROM) in the part concerning signal arrangement of it is attained.

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—EXAMPLE

[Example] Hereafter, it explains, referring to a drawing about the example of this invention. Drawing 1 is the non-encoding signal plot plan common to 16QAM and 64QAM made based on signal arrangement of QPSK. This signal arrangement technique is as stating below.
[0013] First, when it takes notice of I axial seat label in signal arrangement of QPSK of drawing 1 (a), Gray code coordinates are 0 and 1. The figure which adds zero before this figure (dotted-line part in drawing (a)), and is set to 00 and 01 is made, and as this figure is inserted, the figure of [becoming Gray code] 10, 00, 01, and 11 is made from the figure which begins from 1. this -- a degree -- assigning on an I-axis Q-axis as a coordinate of high 16QAM of a dimension, signal arrangement of a symbol location arranges what combined the figure of an I-axis Q-axis by turns (drawing 1 (b)). As for four main symbols, the arrangement as which all patterns are expressed 2 bits of low order by 00 can be taken by doing in this way, as for 2 bits of high orders.
[0014] The thing made to extend to 64QAM by the same technique is shown in drawing 2 . If this is seen, 4 bits of low order of the part enclosed with the dotted line in drawing will serve as Gray code signal arrangement of 16QAM. Moreover, if it sees about 2 bits of low order, four symbols near a core will serve as signal arrangement of QPSK. Thus, it is not based on a modulation technique but signal arrangement can be shared between using the number of bits which suited the modulation technique from the lower bit.
[0015] Similarly, 256QAM and the escape beyond it are also possible, and the method not more than it (QPSK16QAM, 64QAM) can share them. Drawing 3 is the signal plot plan which took the arrangement which 2 bits of high orders come out of main 4 SHISHIBORU, and all patterns come out of 2 bits of low order by 11 in drawing 1 of common to 16QAM and 64QAM not encoding. Drawing 4 shows the signal arrangement which extended signal arrangement of drawing 3 further.
[0016] Drawing 5 is the process in which the signal plot plan of coding common to 16QAM-TCM and 64QAM-TCM is created by making signal arrangement of drawing 1 into a subset. This is applied to signal arrangement of 64QAM-TCM as a subset that drawing 5 (a) in which signal arrangement was carried out by the technique of drawing 1 is not encoded (drawing 5 (b)), while other three subsets rotate 90 degrees at a time, it is arranged, it adds the coding bits 00, 01, 10, and 11 to each from low order, and a signal plot plan is carried out to it (drawing 6).
[0017] If it does in this way, in signal arrangement of drawing 6 , mapping of 4x4 by the side of the core of a shaft (inside of the dotted line in drawing) is 16QAM-TCM, and the distance of the symbols which form a subset can take the distance as before. Signal arrangement possible [256 QAM-TCM and the escape beyond it] and common to the method not more than it (64QAM, 16QAM, QPSK) can be made by the same technique.
[0018] Thus, by not depending signal arrangement and unifying it into a modulation technique, the ROM memory of trellis coding decode equipment as shown in drawing 7 (a), (b), and (c) is reducible.
[0019] Drawing 7 (a) is the block diagram showing the configuration of drawing 5 and the trellis coding equipment using signal arrangement of drawing 6 . A coding bit collapses the information symbol which consists of a non-encoding bit and a coding bit, and after being inputted into an encoder 01 and encoding, it is inputted into the signal arrangement distributor 02. Although the

output by which signal arrangement distribution were carried out is transmitted in the signal arrangement distributor 02, even if it does not prepare signal arrangement distribution ROM about 16QAM, 64QAM, and each 256QAM, signal arrangement distribution ROM can use the same thing by using signal arrangement of drawing 5 and drawing 6 according to the input number of bits.

[0020] Drawing 7 (b) is the block diagram showing the configuration of the trellis decode equipment by representation symbol detection. Input signals Id and Qd are divided into a non-encoding bit and a coding bit, a non-encoding bit is inputted into the representation symbol detector 03, and a hard decision is carried out for every subbit. In the representation symbol detector 03, 6 bit x4 of representation symbols judged subset is outputted. The output is delayed in a shift register 04 until a coding bit is decoded.

[0021] On the other hand, a coding bit is powerfully decoded by the Viterbi decoder 06 using the count result by BMU(branch metric unit) 08. While the decode output outputted from this Viterbi decoder 06 is outputted to the output section, it is collapsed in order to choose a non-encoding bit, and recoding is carried out with an encoder 07. On the other hand, the output of a shift register 04 is inputted into the non-encoding bit selector 05. the non-encoding bit selector 05 -- setting -- the point -- collapsing -- the representation symbol corresponding to the coding bit by which recoding was carried out is chosen, and it is outputted as decode data after that.

[0022] In addition, he uses only 2 bits only of low order of a non-encoding bit, and is trying to use [in the case of 16QAM-TCM] only 4 bits only of non-encoding bit low order at this time in the case of 64QAM-TCM.

[0023] Since according to the above configuration it does not depend on the value of a modulation but a symbol can be detected from the same signal arrangement in the case of representation symbol detection, ROMs are reducible. Drawing 7 (c) is the block diagram by field judging showing the configuration of trellis decode equipment. Input signals Id and Qd are divided into a non-encoding bit and a coding bit, and a non-encoding bit is inputted into the field judging machine 13. This field judging machine 13 judges and outputs the field of an input signal. It goes into a shift register 14 and the output is delayed until a coding bit is decoded.

[0024] On the other hand, while a coding bit is powerfully decoded by the Viterbi decoder 16 and is outputted to the output section using the count result by BMU(branch metric unit) 18, in order to choose a non-encoding bit, recoding of it is carried out with the convolutional code-ized vessel 17. On the other hand, the output of a shift register 14 is inputted into the non-encoding bit selector 15. the non-encoding bit selector 15 -- setting -- the point -- collapsing -- the representation symbol corresponding to the coding bit by which recoding was carried out is chosen, and it is outputted as decode data after that.

[0025] In addition, at this time, in the case of 16QAM-TCM, only 2 bits only of low order of a non-encoding bit are used, and, in the case of 64QAM-TCM, only 4 bits only of non-encoding bit low order are used. Since it does not depend on the value of a modulation but a field judging can be carried out from the same signal arrangement until it results [from a field judging] in a non-encoding bit decoder according to the above configuration, ROMs are reducible.

[0026] As described above, from the coordinate of the I-axis in signal arrangement of QPSK, and each Q-axis, the signal configuration method of this invention extends a Gray code coordinate so that all patterns may come out from a lower bit to the core of a shaft, and makes it a summary to have the signal arrangement same from QPSK to 256QAM by that I and the technique of combining the figure of a Q-axis by turns.

[0027] Namely, a coding means by which the signal arrangement equipment by the side of coding of this invention encodes the coding bit of an information symbol, It has the signal arrangement distribution means which considers the non-encoding bit of the coding output of said coding means, and said information symbol as an input. With said signal arrangement distribution means 0 is added and extended to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit. the figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 -- making -- this -- a degree -- an escape is further recommended as a coordinate of an I-axis and a Q-axis, and it is characterized by making signal arrangement into the subset which has arranged the figure of an I-axis Q-axis

using alternation.
[0028] Moreover, when the coding bit of an information symbol is encoded and the signal arrangement distribution of the non-encoding bit of this coding output and said information symbol are carried out, the decode equipment of this invention 0 is added and extended to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. this -- a degree -- with the means which recommends an escape further as a coordinate of an I-axis and a Q-axis, makes signal arrangement the subset which has arranged the figure of an I-axis Q-axis using alternation, receives such an input signal, and is divided into said non-encoding bit and a coding bit A decode means to decode said divided coding bit, and a representation symbol detection means to consider said divided non-encoding bit as an input, and to detect the symbol, A delay means by which it is delayed until said coding bit is decoded with said decode means in the output of said representation symbol detection means, It has the non-encoding bit selector which chooses a non-encoding bit by considering as an input the coding bit decoded with the output of said delay means, and said decode means. In case the representation symbol of a non-encoding bit is detected, said representation symbol detection means is equipped with the representation symbol detector share-ized to said two or more modulation techniques.
[0029] Moreover, when the coding bit of an information symbol is encoded and the signal arrangement distribution of the non-encoding bit of this coding output and said information symbol are carried out, the decode equipment of this invention 0 is added and extended to the high order bit of the coordinates 0 and 1 of QPSK as an extension bit. The figure which set a high order bit which differs from the figure which adjoins the both sides of the made figures 00 and 01 only 1 bit to 1 is made. this -- a degree -- with the means which recommends an escape further as a coordinate of an I-axis and a Q-axis, makes signal arrangement the subset which has arranged the figure of an I-axis Q-axis using alternation, receives such an input signal, and is divided into said non-encoding bit and a coding bit A decode means to decode said divided coding bit, and a field judging means to consider said divided non-encoding bit as an input, and to judge the field on signal arrangement, A delay means by which it is delayed until said coding bit is decoded with said decode means in the output of said field judging means, It has a decode means to decode a non-encoding bit by considering the output and said decoded coding bit of said delay means as an input. As said field judging means In case the non-encoding bit as an output of said delay means is decoded using the output by which coding decode was carried out, the field judging machine share-ized to two or more modulation techniques is used.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing non-encoding mapping of the Gray code concerning one example of this invention.
[Drawing 2] Drawing showing the extended example of non-encoding mapping of drawing 1 .
[Drawing 3] Drawing showing non-encoding mapping of the Gray code concerning other examples of this invention.
[Drawing 4] Drawing showing the extended example of non-encoding mapping of drawing 3 .
[Drawing 5] Drawing showing mapping common to 16QAM of the Gray code concerning the example of further others of this invention, and 64QAM.
[Drawing 6] Drawing showing the extended example of mapping of drawing 5 .
[Drawing 7] Each block diagram of the trellis coding equipment concerning this invention, the trellis decode equipment which detects a non-encoding symbol as a representation symbol and carries out a double sign, and the trellis decode equipment which carries out a field judging and decodes a non-encoding symbol.
[Drawing 8] Drawing showing conventional non-encoding mapping of Gray code and conventional trellis coding mapping.
[Drawing 9] Trellis decode equipment using the conventional representation symbol detection.
[Drawing 10] The sign mapping Fig. shown in order to explain the conventional method.
[Description of Notations]
01, 07, 17 [-- A shift register, 05 / -- 06 A non-encoding bit selector, 16 / -- The Viterbi decoder 15 / -- 08 A non-encoding bit decoder, 18 / -- BMU (branch metric unit).] -- It collapses and is an encoder and 02. -- A signal arrangement distributor, 03 -- 04 A representation symbol detector, 14

[Translation done.]

引用文献3

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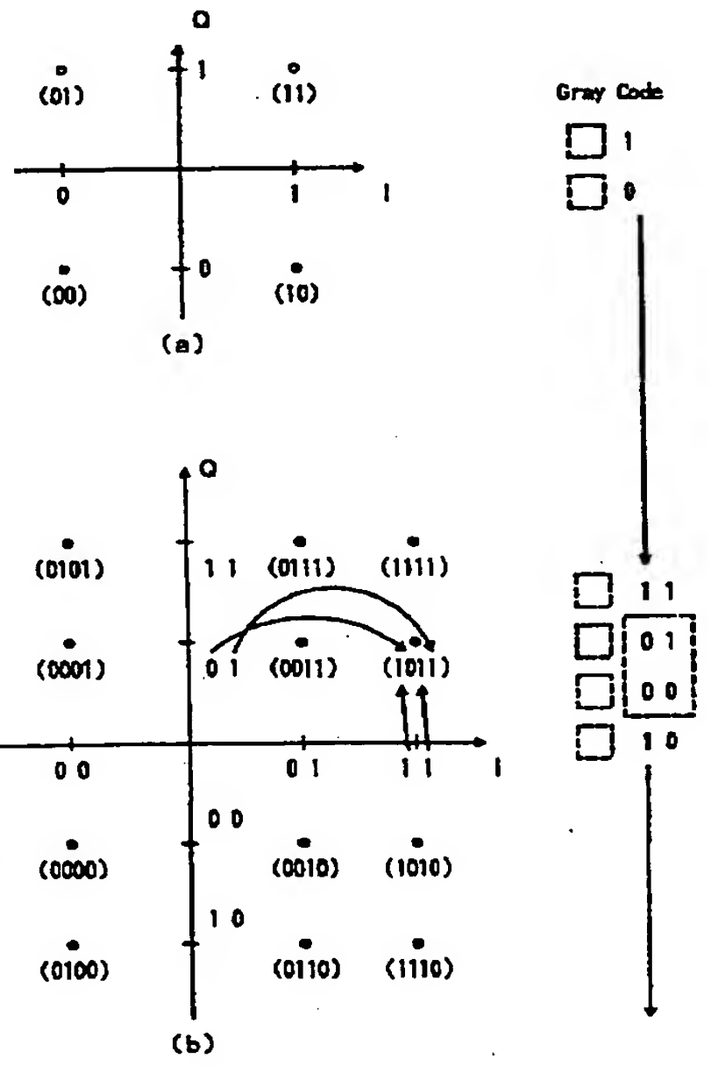
(54)【発明の名称】　伝送方式及び送信受信装置

(57)【要約】
【目的】Ｉ軸Ｑ軸のシンボルの信号配置において座標軸中心に下位ビットからすべてのパターンが出るように配置することにより、複数の変調の値に対応した信号配置を実現することができ符号化のためのＲＯＭを小さくする。
【構成】送信側で符号化変調の信号配置を施す信号配置方式において、信号配置が、ＱＰＳＫの信号配置におけるＩ軸Ｑ軸それぞれの座標のグレイコードをマザーとして、座標軸中心に下位ビットからすべてのパターンがでるように拡張してグレイコード座標を作り、そのＩ軸Ｑ軸のグレイコード座標のビットを交互に組み合わせて作り配置するようにしている。



【特許請求の範囲】

【請求項１】デジタル信号を変復調する伝送方式において、

送信側で信号配置を施し変調する際に、その信号配置は、ＱＰＳＫの信号配置におけるＩ軸Ｑ軸それぞれの座標のグイレイコードをマザーとして、座標軸中心に下位ビットからすべてのパターンがでるように拡張してグレイコード座標を作り、そのＩ軸、Ｑ軸のグレイコード座標のビットを交互に組み合わせて作られることを特徴とし、受信側では復調して、前記信号配置に基づいて信号配置復号を行うことを特徴とした伝送方式。

【請求項２】トレリス符号化変調（以下ＴＣＭと記す）復号の伝送方式において、

送信側では、信号配置は、ＱＰＳＫの信号配置におけるＩ軸Ｑ軸それぞれの座標のグイレイコードをマザーとして、座標軸中心に下位ビットからすべてのパターンがでるように拡張してグレイコード座標を作り、そのＩ軸、Ｑ軸のグレイコード座標のビットを交互に組み合わせて作られており、各サブセットの非符号化ビットの信号配置として変調し、受信側で復調した復調出力を前記信号配置を用いて復号することを特徴とする伝送方式。

【請求項３】情報シンボルの符号化ビットが符号化される符号化手段と、

前記符号化手段の出力と前記情報シンボルの非符号化ビットを入力とする信号配置分配手段と、

前記信号配置された信号を変調する変調手段とを有し、

伝送する際には、前記際信号配置分配手段では、ＱＰＳＫの座標０と１の上位ビットに拡張ビットとして０を負かし、できた数字００、０１の両側に、隣り合う数字と１ビットしか違わないような上位ビットを１とした数字を作り、これを次なるＩ軸、Ｑ軸の座標としてさらに拡張をすすめ、信号配置はＩ軸Ｑ軸の数字を交互に使って配置したサブセットを有することを特徴とした送信装置。

【請求項４】前記拡張ビットを１として拡張することを特徴とする請求項３記載の送信装置。

【請求項５】送信装置では、

情報シンボルの符号化ビットが符号化される符号化手段と、

前記符号化手段の出力と前記情報シンボルの非符号化ビットを入力とする信号配置分配手段と、

前記信号配置された信号を変調する変調手段とを有し、

伝送する際には、前記際信号配置分配手段では、ＱＰＳＫの座標０と１の上位ビットに拡張ビットとして０を付加し、できた数字００、０１の両側に、隣り合う数字と１ビットしか違わないような上位ビットを１とした数字を作り、これを次なるＩ軸、Ｑ軸の座標としてさらに拡張をすすめ、信号配置はＩ軸Ｑ軸の数字を交互に使って配置したサブセットを有し、

前記変調手段で変調され送信された送信信号を受信するに際して、

前記受信信号を復調する復調手段と、

前記復調手段で復調された復調出力を非符号化ビット及び符号化ビットに分け、分けられた前記符号化ビットを復号する復号手段と、

分けられた前記非符号化ビットを入力とし、その代表シンボルを検出する代表シンボル検出手段と、

前記代表シンボル検出手段の出力を前記符号化ビットが前記復号手段で復号されるまで遅延する遅延手段と、

前記遅延手段の出力と前記復号手段により復号された符号化ビットを入力として非符号化ビットを選ぶ、非符号化ビットセレクタとを有し、

前記非符号化ビットの代表シンボルを検出する際、前記代表シンボル検出手段は、複数の変調方式に対して共有化された代表シンボル検出手段であることを特徴とする受信装置。

【請求項６】送信装置では、

情報シンボルの符号化ビットが符号化される符号化手段と、

前記符号化手段の出力と前記情報シンボルの非符号化ビットを入力とする信号配置分配手段と、

前記信号配置された信号を変調する変調手段とを有し、

伝送する際には、前記際信号配置分配手段では、ＱＰＳＫの座標０と１の上位ビットに拡張ビットとして０を負かし、できた数字００、０１の両側に、隣り合う数字と１ビットしか違わないような上位ビットを１とした数字を作り、これを次なるＩ軸、Ｑ軸の座標としてさらに拡張をすすめ、信号配置はＩ軸Ｑ軸の数字を交互に使って配置したサブセットを有し、

前記変調手段で変調され送信された送信信号を受信するに際して、

前記受信信号を復調する復調手段と、

前記復調手段で復調された復調出力を非符号化ビット及び符号化ビットに分け、分けられた前記符号化ビットを復号する復号手段と、

前記復調出力を入力とし、その信号の信号配置上の領域を判定する領域判定手段と、

前記領域判定手段の出力を前記符号化ビットが復号されるまで遅延する遅延手段と、

前記遅延手段の出力と前記復号された符号化ビットを入力として非符号化ビットを復号する復号装置とを有し、

前記受信信号の領域を判定する際、前記領域判定手段は、複数の変調方式に対して共有化した領域判定手段を具備することを特徴とする受信装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明はデジタル変調において多値符号化変調及び復号装置に用いて有効な伝送方式及び送信受信装置に関する。

【０００２】

【従来の技術】現在、多値の変調シンボルの信号配置方法としては、図８（ａ）に示すように、軸座標を１ビットしか違わないようにグレイコード配置した後で、Ｉ軸座標の後にＱ軸座標を記述するという配置方法をとっている。

【０００３】また、誤り訂正をするためにトレリス符号化された符号化変調シンボルの信号配置は、図８（ｂ）に示すように復号の際、硬判定する非符号化ビットを、符号化ビットが同一となるグループ（サブセット）に分けた時に（図中の白丸印等）、それぞれのサブセット内のシンボル間距離が最大となるような配置を変調の値ごとにとる。そのため、たとえばトレリス復号硬判定の代表シンボル検出の際は、図９に示すように１６ＱＡＭ－ＴＣＭ（ＴＣＭ：トレリス符号化変調）では２ビット×４サブセット＝８ビット、６４ＱＡＭ－ＴＣＭでは４ビット×４サブセット＝１６ビット、２５６ＱＡＭ－ＴＣＭでは６ビット×４サブセット＝２４ビットの代表シンボルを変調の値ごとにそれぞれ違う信号配置を決定していた。

【０００４】即ち、図９の復号システムの動作を、図１０（ａ）、図１０（ｂ）の信号配置図を参照して説明することにする。例えば、１６ＱＡＭ－ＴＣＭで伝送したシンボルが受信されたものを図１０の黒丸で示している。

【０００５】受信シンボルは、受信側で図９に示すように代表シンボル検出器８０１～８０３側とＢＭＵ（ブランチメトリックユニット）８０７側に分かれる。代表シンボル検出器は、非符号化ビット（上位２ビット）決定ユニットであり、ＢＭＵ８０７は符号化ビット（下位２ビット）決定ユニットである。

【０００６】代表シンボル検出器、例えば８０１は、図１０（ｂ）に示すように各サブセット毎で受信シンボルに一番近いものを代表シンボルとして決定していく。一方、符号化ビット（下位２ビット）は強力に復号されることから、送信信号はその復号された符号化ビットをもつサブセットの代表シンボルで決定される。代表シンボルは、セレクタ８０４を介してシフトレジスタ８０５に供給される。このシフトレジスタ８０５においては、４つのサブセット毎の代表シンボル（上位２ビット）の４×２ビットを符号化ビットが復号されるまでのビタビ復号遅延分遅延させる。

【０００７】一方、符号化ビット側である、ＢＭＵ８０７においては、各サブセットの代表シンボルに対するブランチメトリックλ０～λ３を計算していく（ブランチメトリック＝各代表シンボルと受信シンボルとの距離：図１０（ｂ）参照）。この計算結果は、ビタビ復号器８０８に入力される。ビタビ復号器８０８では、先の計算結果を用いてたたみ込み符号化の構成で決まる可能な伝送系列からの誤差を累積してパスメトリックとする。このパスメトリックのパスのうち最も確からしいパスの最

過去ビット（パスメモリ中の最過去ビット）がビタビ復号ビットとして出力される（この復号出力は高い信頼性がある）。ビタビ復号結果は、送信側でたたみ込み符号化する前の結果、即ち１ビットの出力となる。しかし、一方では非符号化ビットを選択しなければならない。よって、再度、たたみ込み符号化器８０９でたたみ込み符号化を行った後、非符号化ビットをセレクタ８０６にて選択している。

【０００８】

【発明が解決しようとする課題】上記した従来の変調シンボルの信号配置は、変調の値によって異なるために、例えばトレリス復号の際、非符号化ビットの復号における代表シンボル検出で、変調の値ごとに違った信号配置から代表シンボルを検出しなくてはならず、ＲＯＭとして大きなメモリを必要としていた。

【０００９】そこでこの発明は信号配置を変調の値に依らず統一させることでメモリを小さくすることができる符号化信号配置装置及び復号装置及び信号処理方法提供することを目的とする。

【００１０】

【課題を解決するための手段】上記目的を達成するためにこの発明の信号配置による伝送方法は、送信側で信号配置を施し変調する際に、その信号配置は、ＱＰＳＫの信号配置におけるＩ軸Ｑ軸それぞれの座標のグイレイコードをマザーとして、座標軸中心に下位ビットからすべてのパターンがでるように拡張してグレイコード座標を作り、そのＩ軸、Ｑ軸のグレイコード座標のビットを交互に組み合わせて作られることを特徴とし、受信側では復調して、前記信号配置に基づいて信号配置復号を行うものである。

【００１１】

【作用】上記のように構成されたものは、さまざまな変調の値に対応した統一の信号配置を実現できるために、信号配置に係る箇所でのメモリ（ＲＯＭ）の小型化が可能となる。

【００１２】

【実施例】以下、この発明の実施例について図面を参照しながら説明する。図１は、ＱＰＳＫの信号配置をもとにして作った１６ＱＡＭ、６４ＱＡＭ共通の、非符号化の信号配置図である。この信号配置手法は、以下に述べるとおりである。

【００１３】まず、図１（ａ）のＱＰＳＫの信号配置においてＩ軸座標に注目するとグレイコード座標は０と１である。この数字の前（図（ａ）中の点線部分）に０を付加して００、０１となる数字を作り、この数字をはさむようにして、１からはじまる数字でグレイコードとなるように１０、００、０１、１１という数字を作る。これを次なる次元の高い１６ＱＡＭの座標としてＩ軸Ｑ軸上に割り振り、シンボル位置の信号配置は、Ｉ軸Ｑ軸の数字を交互に組み合わせたものを配置する（図１

（ｂ））。このようにすることで中心の４シンボルは、上位２ビットは００で下位２ビットはすべてのパターンが表現される配置をとることができる。

【００１４】同様な手法により６４ＱＡＭまで拡張させたものを図２に示す。これを見ると図中の点線で囲った部分の下位４ビットは１６ＱＡＭのグレイコード信号配置となる。また下位２ビットについて見ると、中心付近の４つのシンボルはＱＰＳＫの信号配置となる。このように下位ビットから変調方式にあったビット数を使用していくことで、変調方式によらず信号配置を共有できる。

【００１５】同様にして２５６ＱＡＭ、それ以上の拡張も可能でそれ以下の方式（ＱＰＳＫ１６ＱＡＭ、６４ＱＡＭ）で共有できる。図３は、図１において中心の４シンボルは上位２ビットが１１で下位２ビットはすべてのパターンがでる配置をとるようにした、１６ＱＡＭ、６４ＱＡＭ共通の非符号化の信号配置図である。図４は図３の信号配置を更に拡張した信号配置を示している。

【００１６】図５は、図１の信号配置をサブセットとして、１６ＱＡＭ－ＴＣＭ、６４ＱＡＭ－ＴＣＭ共通の符号化の信号配置図の作成される過程である。これは、図１の手法により信号配置された図５（ａ）を非符号化のサブセットとして６４ＱＡＭ－ＴＣＭの信号配置にあてはめ（図５（ｂ））、他の３つのサブセットも９０°ずつ回転させながら配置してゆき、それぞれに符号化ビット００、０１、１０、１１を下位から付加して信号配置図されたものである（図６）。

【００１７】このようにすると、図６の信号配置において、軸の中心側（図中の点線内）の４×４のマッピングは１６ＱＡＭ－ＴＣＭであり、サブセットを形成するシンボル同士の距離は今までどおりの距離がとれるようになっている。同じ手法により２５６ＱＡＭ－ＴＣＭ、それ以上の拡張が可能でそれ以下の方式（６４ＱＡＭ、１６ＱＡＭ、ＱＰＳＫ）共通の信号配置を作ることができる。

【００１８】このように信号配置を変調方式に依らず統一させることで、図７（ａ）、（ｂ）、（ｃ）に示すようなトレリス符号化復号装置のＲＯＭメモリを削減することができる。

【００１９】図７（ａ）は、図５、図６の信号配置を利用したトレリス符号化装置の構成を示すブロック図である。非符号化ビット、符号化ビットで構成される情報シンボルは、符号化ビットがたたみ込み符号化器０１に入力され符号化された後、信号配置分配器０２に入力される。信号配置分配器０２では、信号配置分配された出力を送信するが、図５、図６の信号配置を用いることで、１６ＱＡＭ、６４ＱＡＭ、２５６ＱＡＭ、それぞれについて信号配置分配ＲＯＭを用意しなくても、信号配置分配ＲＯＭは、入力ビット数に応じて同じものを用いることができる。

【００２０】図７（ｂ）は、代表シンボル検出によるトレリス復号装置の構成を示すブロック図である。受信信号Ｉｄ、Ｑｄは非符号化ビット、及び符号化ビットに分けられ、非符号化ビットは代表シンボル検出器０３へ入力されサブビットごとに硬判定される。代表シンボル検出器０３では、判定された代表シンボル６ビット×４サブセットを出力する。その出力は、符号化ビットが復号されるまでの間シフトレジスタ０４において遅延される。

【００２１】一方、符号化ビットは、ＢＭＵ（ブランチメトリックユニット）０８による計算結果を用いて、ビタビ復号器０６により強力に復号される。このビタビ復号器０６より出力された復号出力は、出力部に出力される一方で、非符号化ビットを選択するためにたたみ込み符号化器０７により再符号化される。他方、シフトレジスタ０４の出力は、非符号化ビットセレクタ０５に入力されている。非符号化ビットセレクタ０５においては、先のたたみ込みにより再符号化された符号化ビットに対応した代表シンボルが選択され、その後、復号データとして出力される。

【００２２】尚、この時、１６ＱＡＭ－ＴＣＭの場合、非符号化ビットの下位２ビットのみ使用し、６４ＱＡＭ－ＴＣＭの場合、非符号化ビット下位４ビットのみ使用するようにしている。

【００２３】以上の構成によれば代表シンボル検出の際、変調の値に依らず同じ信号配置よりシンボルを検出できるため、ＲＯＭを削減することができる。図７（ｃ）は、領域判定による、トレリス復号装置の構成を示すブロック図である。受信信号Ｉｄ、Ｑｄは非符号化ビット、及び符号化ビットに分けられ、非符号化ビットは、領域判定器１３へ入力される。この領域判定器１３は、受信信号の領域を判定し出力する。その出力は、符号化ビットが復号されるまでの間シフトレジスタ１４に入り遅延される。

【００２４】一方、符号化ビットは、ＢＭＵ（ブランチメトリックユニット）１８による計算結果を用いて、ビタビ復号器１６により強力に復号され、出力部に出力される一方で、非符号化ビットを選択するために畳み込み符号化器１７により再符号化される。他方、シフトレジスタ１４の出力は、非符号化ビットセレクタ１５に入力されている。非符号化ビットセレクタ１５においては、先のたたみ込みにより再符号化された符号化ビットに対応した代表シンボルが選択され、その後、復号データとして出力される。

【００２５】尚この時、１６ＱＡＭ－ＴＣＭの場合非符号化ビットの下位２ビットのみ使用し、６４ＱＡＭ－ＴＣＭの場合非符号化ビット下位４ビットのみ使用する。以上の構成によれば領域判定から非符号化ビットデコーダに至るまで、変調の値に依らず同じ信号配置より領域判定できるため、ＲＯＭを削減することができる。

【００２６】上記したようにこの発明の信号配置方法は、ＱＰＳＫの信号配置における Ｉ軸、Ｑ軸それぞれの座標から、軸の中心に下位ビットからすべてのパターンが出るようにグレイコード座標を拡張して、そのＩ、Ｑ軸の数字を交互に組み合わせる手法によりＱＰＳＫから２５６ＱＡＭまで同一の信号配置を有することを要旨とする。

【００２７】即ちこの発明の符号化側の信号配置装置は、情報シンボルの符号化ビットを符号化する符号化手段と、前記符号化手段の符号化出力と前記情報シンボルの非符号化ビットを入力とする信号配置分配手段とを有し、前記信号配置分配手段では、ＱＰＳＫの座標０と１の上位ビットに拡張ビットとして０を付加して拡張し、できた数字００、０１の両側に、隣り合う数字と１ビットしか違わないような上位ビットを１とした数字を作り、これを次なるＩ軸、Ｑ軸の座標としてさらに拡張をすすめ、信号配置はＩ軸Ｑ軸の数字を交互に使って配置したサブセットとすることを特徴とする。

【００２８】またこの発明の復号装置は、情報シンボルの符号化ビットが符号化されており、この符号化出力と前記情報シンボルの非符号化ビットが信号配置分配されるときに、ＱＰＳＫの座標０と１の上位ビットに拡張ビットとして０を付加して拡張し、できた数字００、０１の両側に、隣り合う数字と１ビットしか違わないような上位ビットを１とした数字を作り、これを次なるＩ軸、Ｑ軸の座標としてさらに拡張をすすめ信号配置はＩ軸Ｑ軸の数字を交互に使って配置したサブセットとしており、このような受信信号を受信して前記非符号化ビットおよび符号化ビットに分ける手段と、分けられた前記符号化ビットを復号する復号手段と、分けられた前記非符号化ビットを入力とし、そのシンボルを検出する代表シンボル検出手段と、前記代表シンボル検出手段の出力を前記符号化ビットが前記復号手段で復号されるまで遅延する遅延手段と、前記遅延手段の出力と前記復号手段で復号された符号化ビットを入力として非符号化ビットを選ぶ非符号化ビットセレクタとを有し、非符号化ビットの代表シンボルを検出する際、前記代表シンボル検出手段は、前記複数の変調方式に対して共有化された代表シンボル検出器を備えるものである。

【００２９】またこの発明の復号装置は、情報シンボルの符号化ビットが符号化されており、この符号化出力と前記情報シンボルの非符号化ビットが信号配置分配されるときに、ＱＰＳＫの座標０と１の上位ビットに拡張ビットとして０を付加して拡張し、できた数字００、０１の両側に、隣り合う数字と１ビットしか違わないような上位ビットを１とした数字を作り、これを次なるＩ軸、Ｑ軸の座標としてさらに拡張をすすめ信号配置はＩ軸Ｑ軸の数字を交互に使って配置したサブセットとしており、このような受信信号を受信して前記非符号化ビットおよび符号化ビットに分ける手段と、分けられた前記符号化ビットを復号する復号手段と、分けられた前記非符号化ビットを入力とし、信号配置上の領域を判定する領域判定手段と、前記領域判定手段の出力を前記符号化ビットが前記復号手段で復号されるまで遅延する遅延手段と、前記遅延手段の出力と前記復号された符号化ビットを入力として非符号化ビットを復号する復号手段を有し、前記領域判定手段としては、符号化復号された出力を用いて、前記遅延手段の出力としての非符号化ビットを復号する際、複数の変調方式に対して共有化された領域判定器が用いられるものである。

【００３０】

【発明の効果】以上説明したようにこの発明によれば信号配置において座標軸中心に下位ビットからすべてのパターンが出るように配置することにより、複数の変調の値に対応した信号配置を実現することができ、ＲＯＭを小さくすることができる。

【図面の簡単な説明】

【図１】この発明の一実施例に係わるグレイコードの非符号化マッピングを示す図。

【図２】図１の非符号化マッピングの拡張例を示す図。

【図３】この発明の他の実施例に係わるグレイコードの非符号化マッピングを示す図。

【図４】図３の非符号化マッピングの拡張例を示す図。

【図５】この発明のさらに他の実施例に係わるグレイコードの１６ＱＡＭ、６４ＱＡＭ共通のマッピングを示す図。

【図６】図５のマッピングの拡張例を示す図。

【図７】この発明に係わるトレリス符号化装置、非符号化シンボルを代表シンボルとして検出して複号するトレリス復号装置、非符号化シンボルを領域判定して復号するトレリス復号装置の各ブロック図。

【図８】従来のグレイコードの非符号化マッピングおよびトレリス符号化マッピングを示す図。

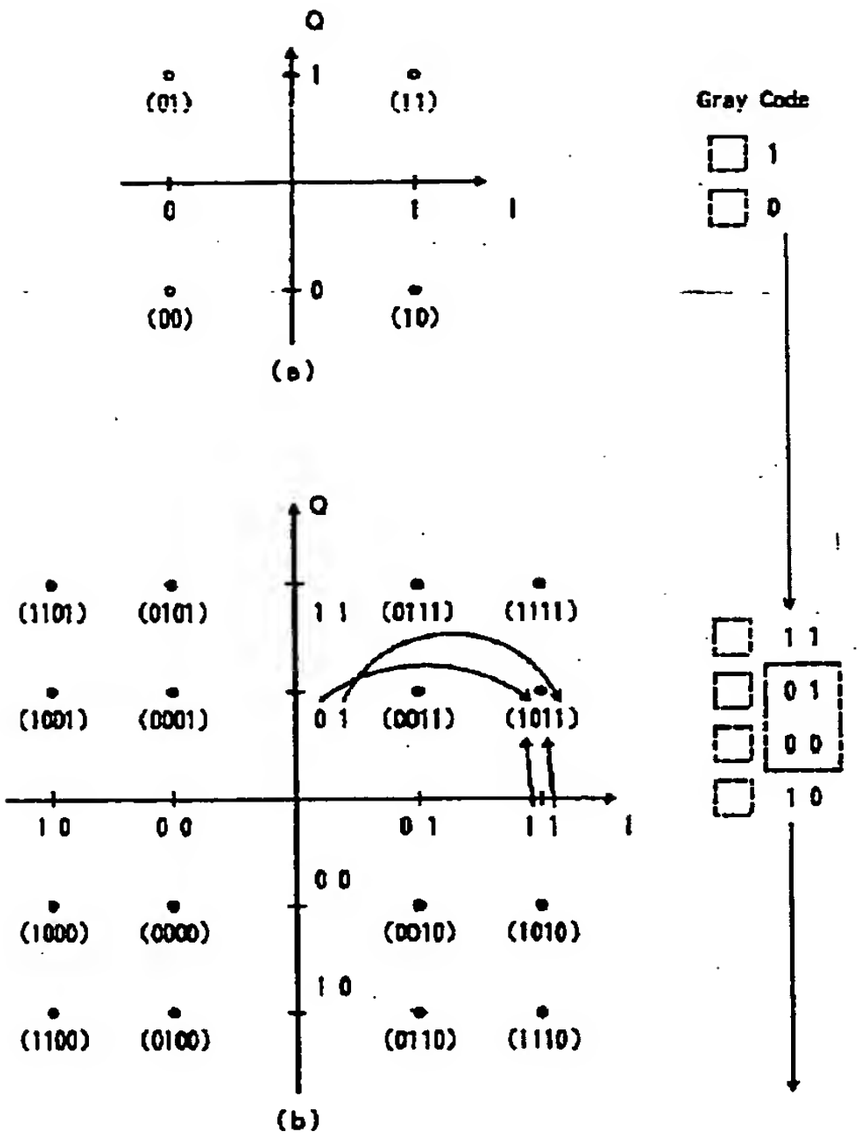
【図９】従来の代表シンボル検出を利用したトレリス復号装置。

【図１０】従来の方式を説明するために示した符号マッピング図。

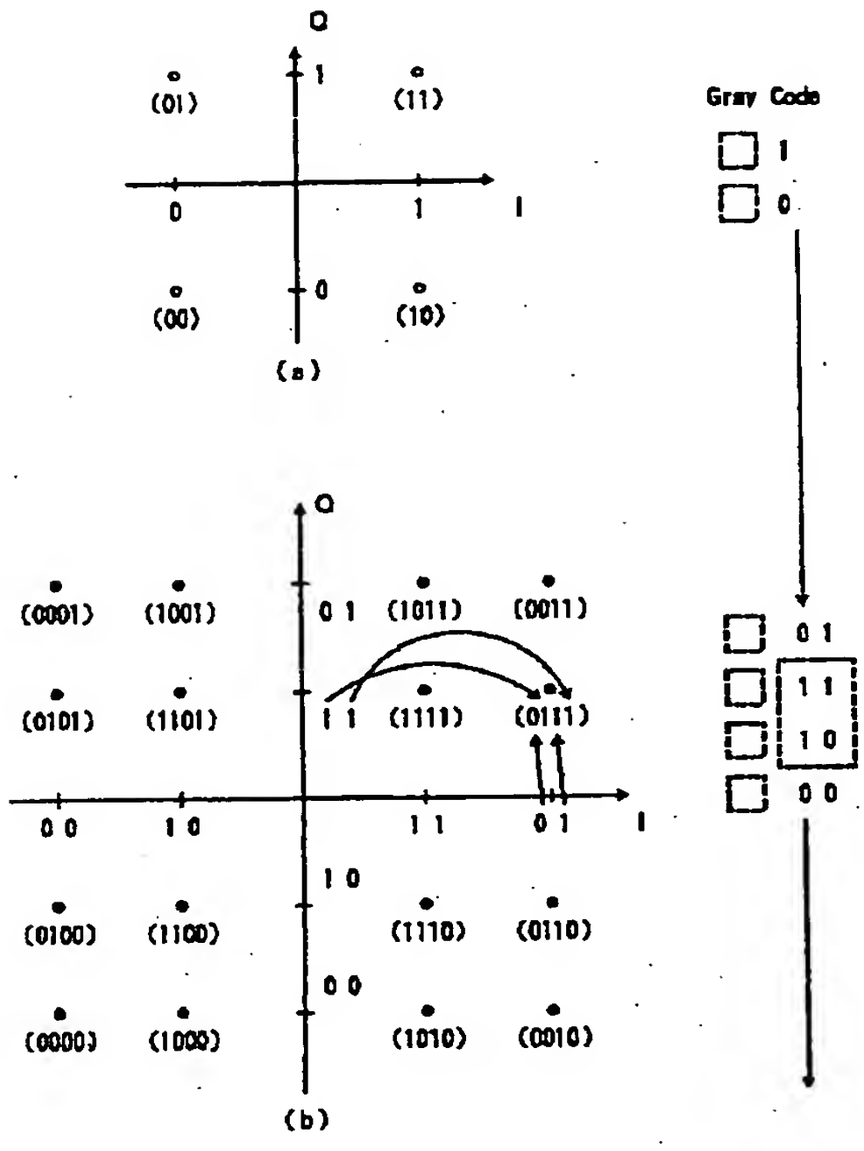
【符号の説明】

０１、０７、１７…たたみ込み符号化器、０２…信号配置分配器、０３…代表シンボル検出器、０４、１４…シフトレジスタ、０５…非符号化ビットセレクタ、０６、１６…ビタビ復号器、１５…非符号化ビットデコーダ、０８、１８…ＢＭＵ（ブランチメトリックユニット）。

【図１】


Q
I
(01)
(11)
(00)
(10)
(a)
Gray Code
1
0
(1101) (0101) (0111) (1111)
(1001) (0001) (0011) (1011)
(1000) (0000) (0010) (1010)
(1100) (0100) (0110) (1110)
(b)

【図３】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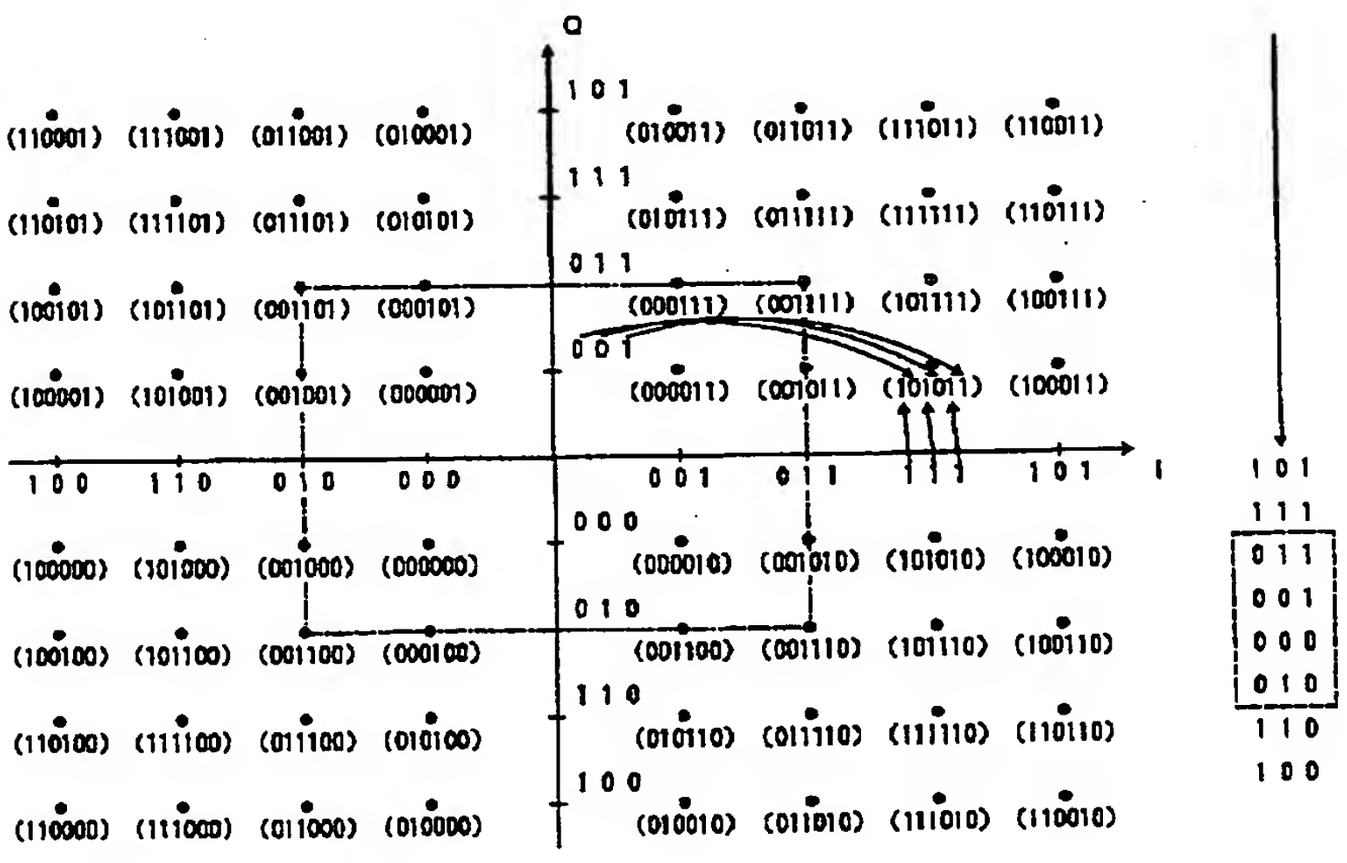
I
(01)
(11)
(00)
(10)
(a)
Gray Code
1
0
(0001) (1001) (1011) (0011)
(0101) (1101) (1111) (0111)
(0100) (1100) (1110) (0110)
(0000) (1000) (1010) (0010)
(b)

【図２】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(110101) (111101) (011101) (010101)
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(100001) (101001) (001001) (000001)
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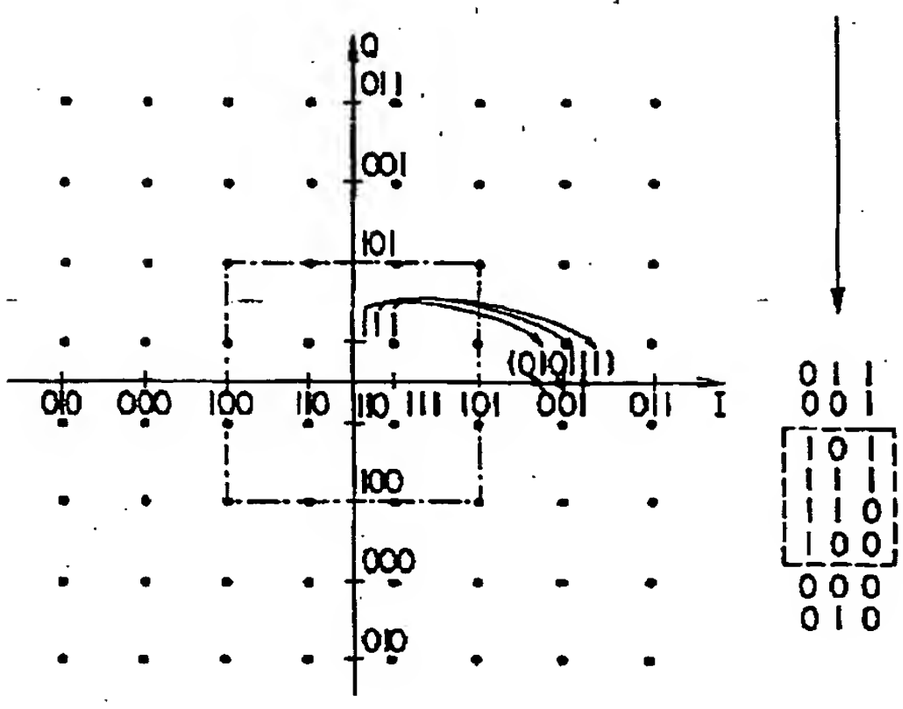
(100100) (101100) (001100) (000100)
(110100) (111100) (011100) (010100)
(110000) (111000) (011000) (010000)
(010011) (011011) (111011) (110011)
(010111) (011111) (111111) (110111)
(000111) (001111) (101111) (100111)
(000011) (001011) (101011) (100011)
(000010) (001010) (101010) (100010)
(001100) (001110) (101110) (100110)
(010110) (011110) (111110) (110110)
(010010) (011010) (111010) (110010)
Gray Code

【図４】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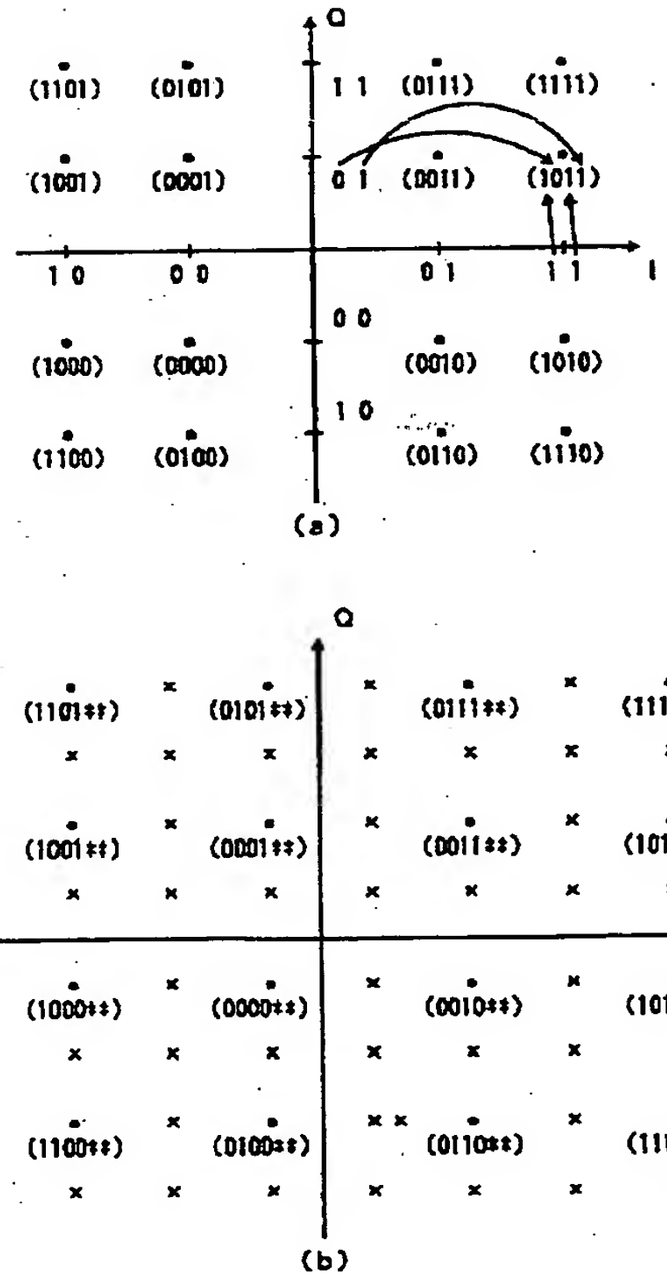
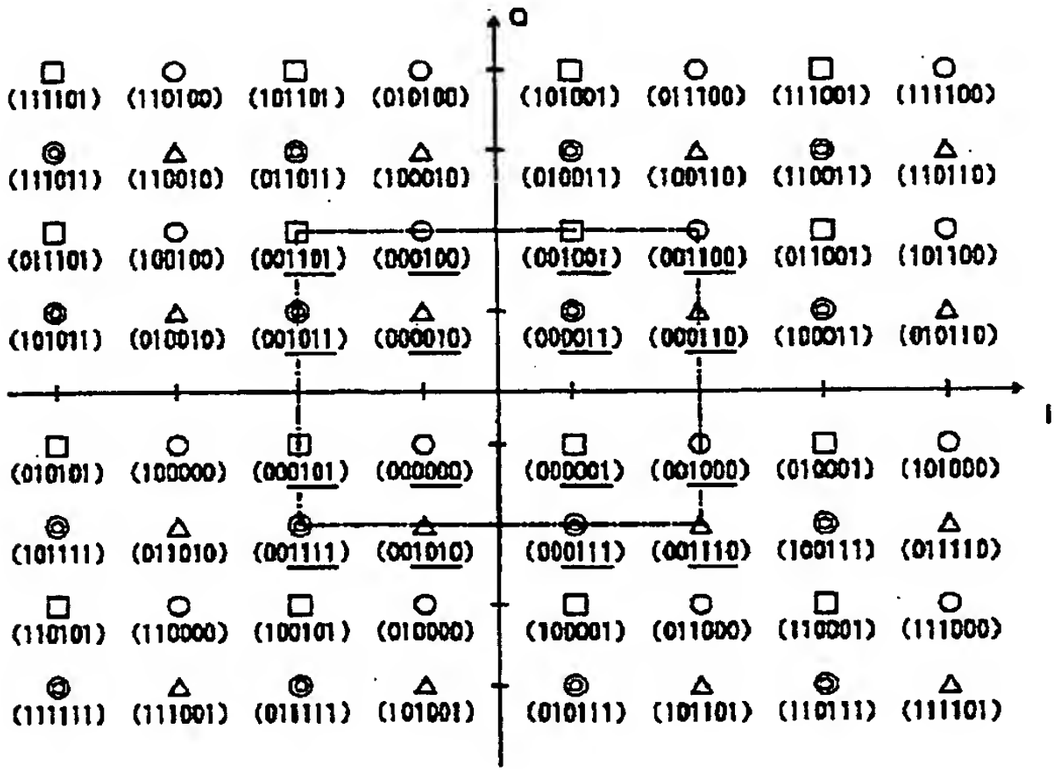
I
(0101)
0 1 1
0 0 1
0 1 0
0 0 0

【図５】


Q
I
(1101) (0101) (0111) (1111)
(1001) (0001) (0011) (1011)
(1000) (0000) (0010) (1010)
(1100) (0100) (0110) (1110)
1 1
0 1
1 0
0 0
(a)
(1101**) (0101**) (0111**) (1111**)
(1001**) (0001**) (0011**) (1011**)
(1000**) (0000**) (0010**) (1010**)
(1100**) (0100**) (0110**) (1110**)
(b)

【図６】


Q
I
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(101011) (010010) (001011) (000010) (000011) (000110) (100011) (010110)
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(101111) (011010) (001111) (001010) (000111) (001110) (100111) (011110)
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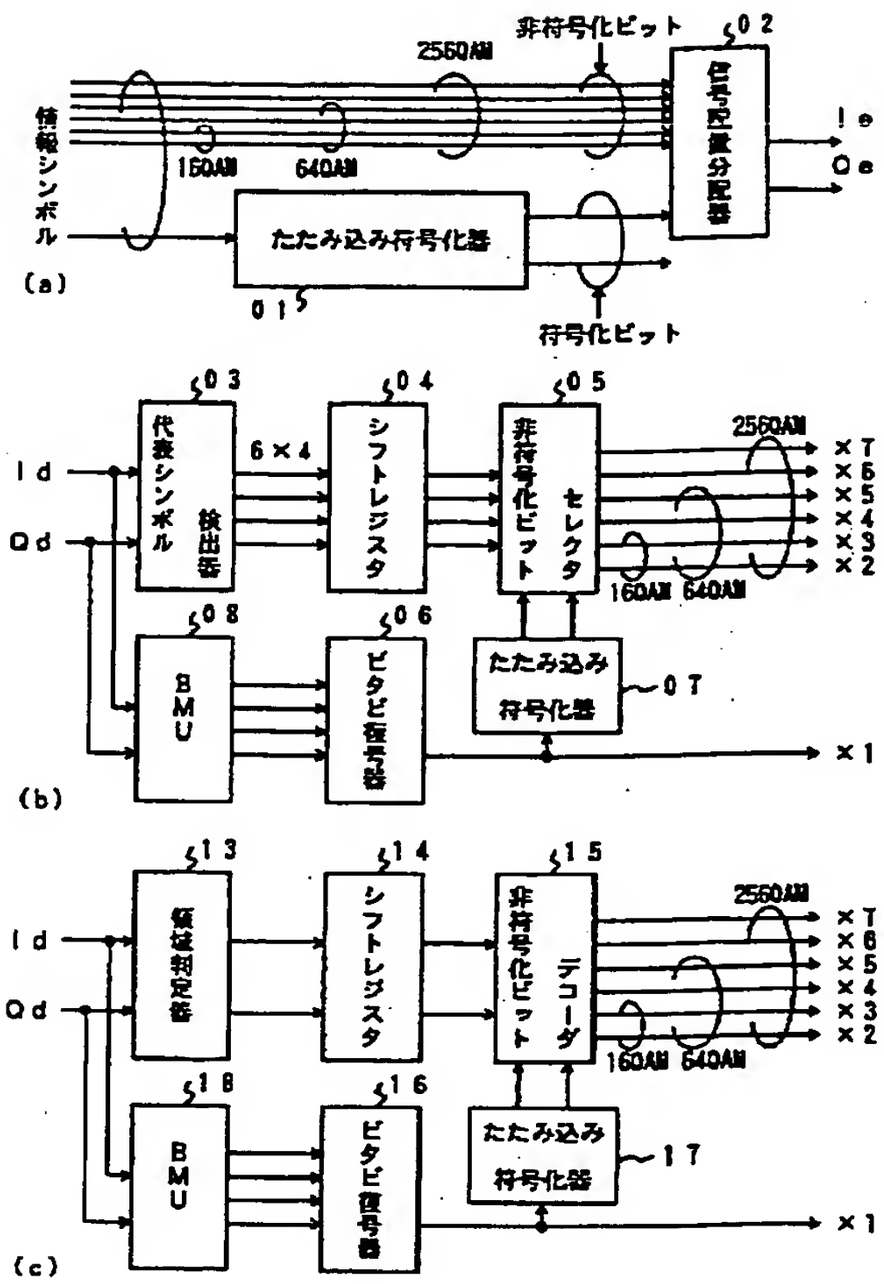
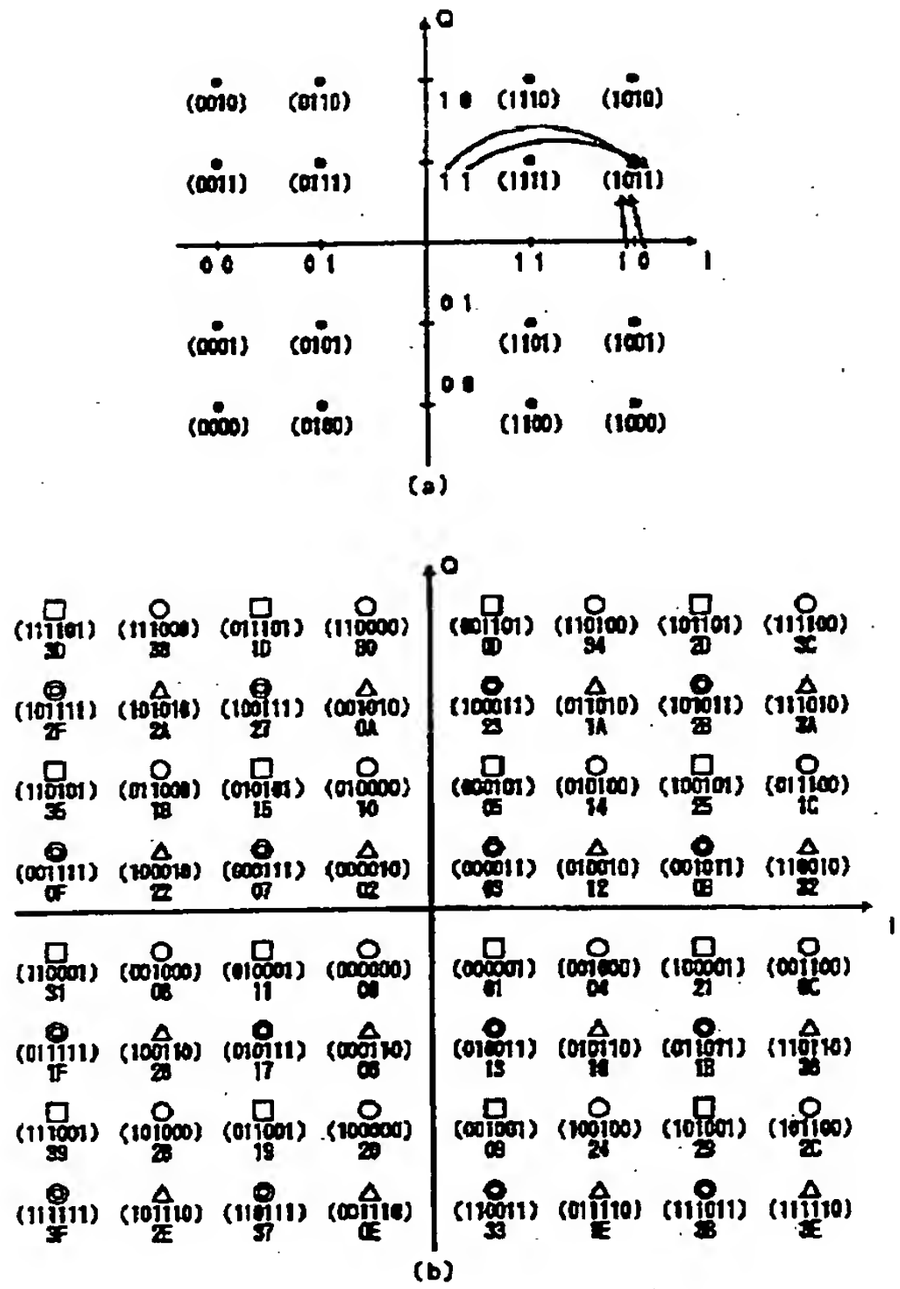
(111111) (111001) (011111) (101001) (010111) (101101) (110111) (111101)

【図７】


非符号化ビット
02
2560AM
情報シンボル
160AM
640AM
信号配置分配器
!e
Qe
たたみ込み符号化器
01
符号化ビット
(a)
03
04
05
代表シンボル検出器
シフトレジスタ
非符号化ビットセレクタ
Id
Qd
6×4
2560AM
×T
×5
×4
×3
×2
160AM 640AM
08
06
07
BMU
ビタビ復号器
たたみ込み符号化器
×1
(b)
13
14
15
領域判定器
シフトレジスタ
非符号化ビットデコーダ
Id
Qd
2560AM
×T
×6
×5
×4
×3
×2
160AM 640AM
18
16
17
BMU
ビタビ復号器
たたみ込み符号化器
×1
(c)

【図８】


Q
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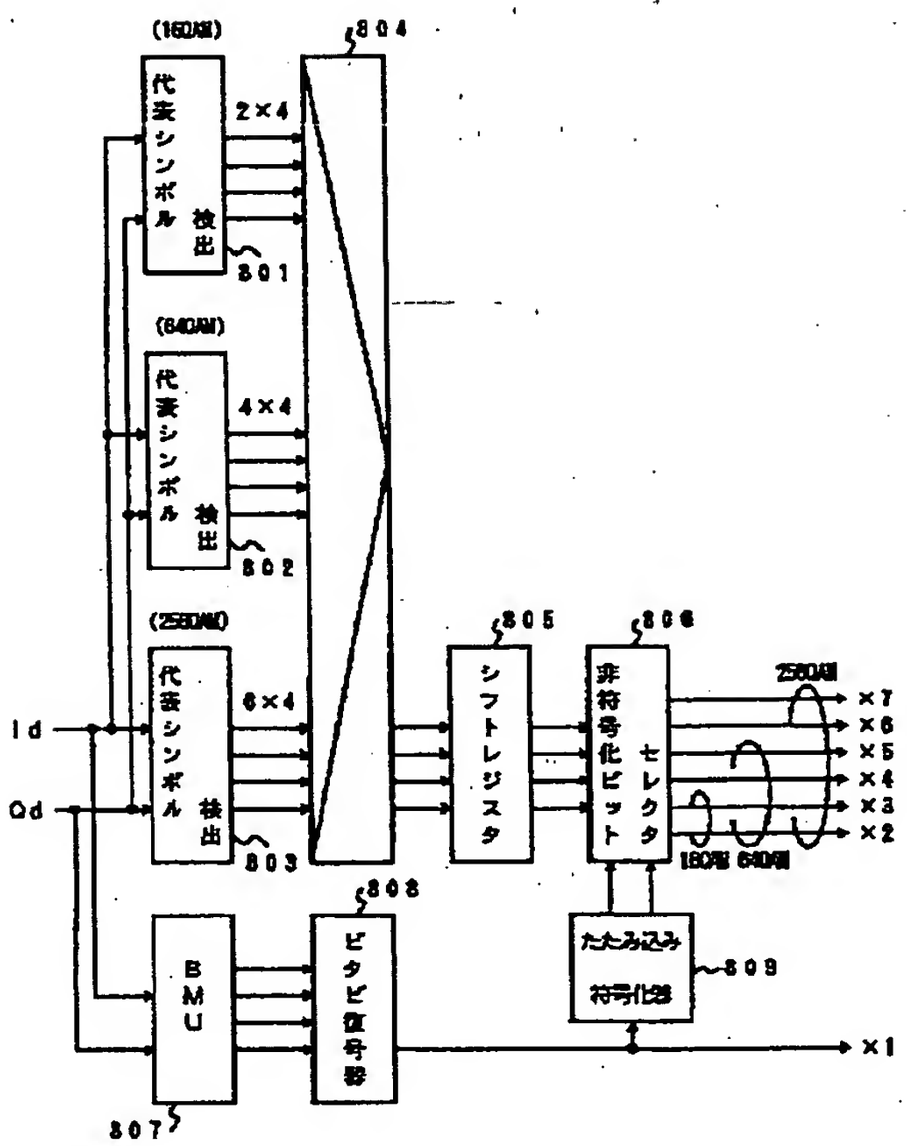
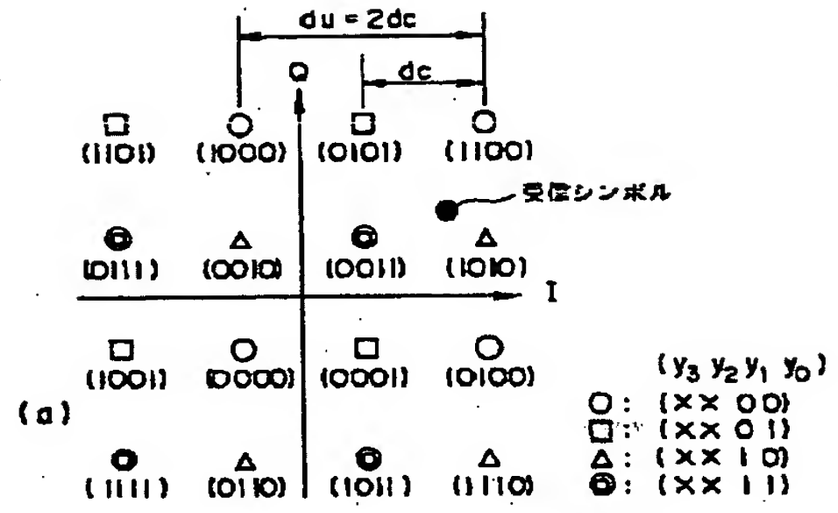
(0011) (0111) 11 (1111) (1011)
00 01 11 10 I
01
(0001) (0101) (1101) (1001)
00
(0000) (0100) (1100) (1000)
(a)
(111101) 3D (111000) 38 (011101) 1D (110000) 18
(101111) 2F (101010) 2A (001111) 07 (001010) 0A
(110101) 35 (011000) 18 (010101) 15 (010000) 10
(001111) 0F (100010) 22 (000111) 07 (000010) 02
(000101) 05 (010100) 14 (100101) 25 (011100) 1C
(000011) 03 (010010) 12 (001011) 0B (110010) 32
(110001) 31 (001000) 08 (010001) 11 (000000) 00
(011111) 1F (100110) 26 (010111) 17 (000110) 06
(111001) 39 (101000) 28 (011001) 19 (100000) 20
(111111) 3F (101110) 2E (011011) 1B (001110) 0E
(000001) 01 (001000) 04 (100001) 21 (001100) 0C
(010011) 13 (010110) 16 (011011) 1B (110110) 36
(001001) 09 (100100) 24 (101001) 29 (101100) 2C
(100011) 23 (011010) 1A (101011) 2B (111010) 3A
I
(b)

【図９】



【図１０】



16QAMのトレリス符号化信号配置図